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AREA AND NOISE OPTIMISED MIXED SIGNAL PLL ARCHITECTURE FOR PORTABLE APPLICATIONS

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ABSTRACT

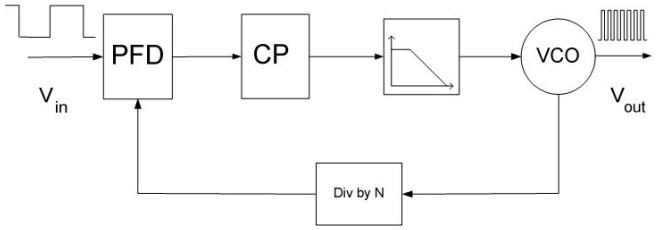
This paper presents low frequency PLL architecture with low noise and less area that has been used in a multi-radio SOC for portable applications. In conventional analog PLL dynamic currents due to charge injection in charge pump circuit would cause significant spur. Large values of resistors involved in charge pump would also produce a large thermal noise that translates into excessive phase noise. Filters which are used in PLL implemented using passive or active components. Large values of resistors in the filters would cause phase noise. In the modified mixed signal architecture allows the active filter to be connected with the closed loop through large value of resistor only for the short period. This avoids leakage of current through resistance back to phase detector intern it reduces spur and phase noises during locking and improves performance. Area of the PLL system is considerably optimized by using modified phase frequency detector.

Keywords- *Clock Generation, Mixed Signal Design, Mentor Graphics Pyxis, Phase Locked Loop (PLL), System On Chip (SOC).*

I. INTRODUCTION

Phase locked loops (PLLs) are widely used for frequency synthesis and clock generation in modern Systems-On-Chip (SOC). A PLL is a control system which uses negative feedback to align the clock phase of a voltage controlled oscillator (VCO) to that of the input reference. Typically a Quartz Crystal Oscillator (XO) is used to generate the input reference. A quartz crystal is a piezo-electric device which produces a mechanical oscillation when a voltage source is applied; the frequency of oscillation is determined by the shape, the cut and the elastic constants of the crystal [2]. Each XO provides a precise, fixed frequency source often in the range of a few kHz to tens of MHz. A higher oscillation frequency is also possible by tuning a crystal to its harmonics, called overtone frequencies. An XO exhibits extremely low phase noise due to its high Q factor, which is several orders of magnitude higher than an LC tank oscillator [3]. An XO also offers superior thermal stability often within 100ppms. However an XO is typically designed around a few standard frequencies. The main advantage of using a PLL for frequency multiplication lies in its ability to synthesize a highly tunable clock source using a local VCO with its in-band phase noise performance approaching that of the XO. A block diagram of a typical PLL is shown in Fig. 1. A phase frequency detector (PFD) or a phase detector (PD) is used to compare the phase between the reference clock and the feedback clock; the phase difference is measured using a charge pump (CP); the CP current is then converted to voltage across the loop filter (LPF)

Figure:**1** A Typical PLL Block Diagram



the voltage signal gets further smoothed out in the LPF and is used to tune the VCO; a divided-down version of the VCO clock feeds back to the PD and the loop is closed. In steady state frequency multiplication is achieved, $f_{vco}=N.f_{ref}$ where N is the divide ratio.

Phase locked loop (PLL) [6], [10], [11] is the heart of the many modern electronics as well as communication system. Recently plenty of the researches have conducted on the design of phase locked loop

(PLL) circuit and still research is going on this topic. Most of the researches have conducted to realize a higher lock range PLL with lesser lock time [4] and have tolerable phase noise. The most versatile application of the phase locked loops (PLL) is for clock generation and clock recovery in microprocessor, networking, communication systems, and frequency synthesizers

The IF signal is further amplified and digitized by an ADC and then subjected to complex digital signal processing to recover the desired signal. The lock signal for the ADC is generally required to have very low phase noise in order to meet tight signal-to-noise requirements.

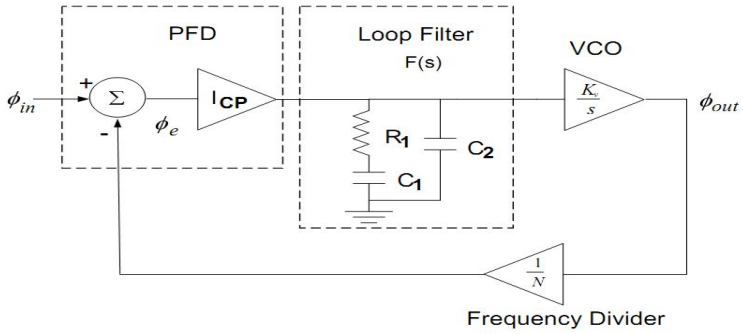
One example of this is the frequency-modulation (FM) transceiver, which is now an integral part of virtually every smart phone. Although a high-frequency crystal oscillator is available on these phones, the FM receiver, which can have long play times, is required to work off of a 32 kHz reference in order to minimize power consumption. The low input frequency limits the loop bandwidth that the PLL can have, which, in turn, makes it very difficult to implement the PLL without external components. This work describes a low frequency PLL architecture that has been used in an FM receiver, which is part of a multi-radio SOC for portable applications [7].

II. PLL ANALYSIS

1. Phase Domain Analysis of Conventional PLL

The PLL is a nonlinear system which poses difficulties for the conventional analysis method of using a transfer function, especially during lock acquisition. However in the locked condition, a linear time-invariant (LTI) model can be used, assuming the PFD transfer characteristic is linear in this operating region [6]. A phase-domain LTI model is shown in Fig. 2, where the PFD is modeled with a linear gain of $I_{CP}/2\pi$ and K_V is the VCO gain in [Hz/V]. The ideal integration 1/s accounts for frequency to phase conversion. Here we have assumed that the VCO response time is much faster than the loop bandwidth, as is typical, and no pole is modeled in the VCO gain. A second order passive loop filter formed by R_1, C_1 and C_2 is used as an example for ease of analysis.

Figure:2 Phase Domain Linearised Model



This is a third order, type II loop with two integrator poles at DC. We approach a third order loop problem with a second order approximation by neglecting the high frequency pole at 1/ (R1C2); this allows for an exact closed-form solution. Note in (1) the 2π factor in the PFD gain is cancelled by the VCO gain given by Kv.2π in [rad/V].

$$H(s) = \frac{2\varsigma\omega_n s + \omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2} \quad (1)$$

By definition we have:

$$\omega_n = \sqrt{\frac{I_{cp}K_v}{NC_1}}$$

$$\varsigma = \frac{1}{2}\sqrt{\frac{I_{cp}K_vC_1}{N}}R_1$$

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Where, ω_n is called the natural frequency of the system. It is the resonant frequency of the un-damped system. ζ is called the damping factor. A damped system prevents excessive peaking. Rewriting the loop gain in terms of the above defined parameters, we have:

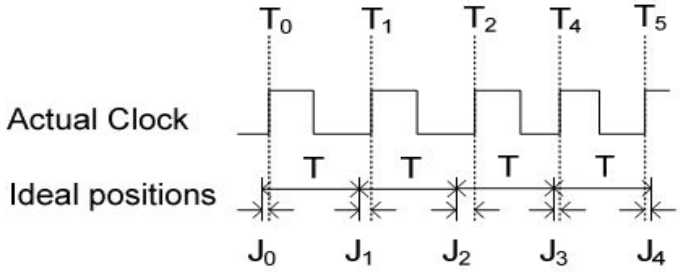
$$G(s) = \frac{2\zeta\omega_n + \omega_n^2}{s^2} \quad (2)$$

The last approximation is used in design to quickly estimate the closed loop bandwidth. It is based on [8]. (4), (5) and (7) are used in design to find the loop filter components. K_V is heavily technology dependent and is usually not a design parameter; it is determined through circuit simulation.

2. Phase Noise And Jitter

Phase noise is a measure for spectral purity of a signal. In the time domain representation, it is the random fluctuation of the phase of a waveform due to timing "Phase noise is a measure for spectral purity of a signal. In the time domain representation, it is the random fluctuation of the phase of a waveform due to timing "jitter". Jitter by definition is the variation of the significant instants of a clock signal from their ideal positions in time. This is also referred to as "total jitter "or "absolute jitter" [5]. jitter". Jitter by definition is the variation of the significant instants of a clock signal from their ideal positions in time. This is also referred to as "total jitter "or "absolute jitter".

Figure:3 Clock jitter

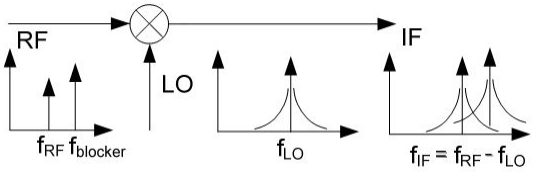


Absolute jitter can be derived from phase noise by integrating the total area under the phase noise curve. The lower integral limit is usually application specific. On the other hand, phase noise can also be derived by taking the power spectral density of jitter, {jn}, assuming {jn} is a stationary stochastic process. Power spectral density is a measure of energy distribution over frequency. For a wide-sense stationary random process, it is defined as the Fourier transform of the autocorrelation function.

3. Effects of Phase Noise and Spur on a System

In modern communication systems PLL synthesizers are frequently used as the local oscillator (LO) signal on the receive side to down convert an RF signal band to IF. The phase noise and spurious performance of the LO signal are particularly important in the receiving path. Excessive phase noise results in reciprocal mixing which limits the receiver sensitivity.

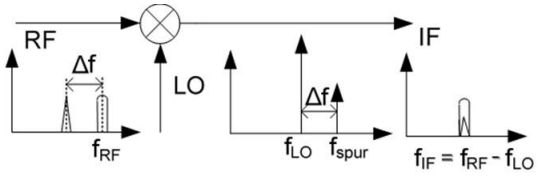
Figure:**4** Reciprocal Mixing



In the process of down conversion, the phase noise of the LO will transfer on to the IF signal, and this is true even if the signal in the RF band is noiseless. This can become worse if a large blocker is present in the vicinity of a small RF signal of interest. The reciprocal noise due to the blocker would dominate the noise at IF. This is illustrated in Fig 4. In addition, the spurs on LO can directly cause channel corruption by mixing two adjacent channels down to the same IF frequency. This happens if a spur tone is located off LO by the same offset Δf as an adjacent channel is displaced in the RF band. This is depicted in Fig. 5 [9]. On the other hand, when

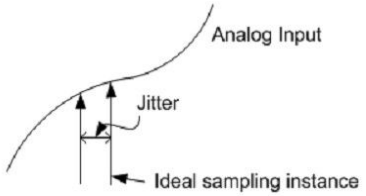
a PLL is used for clock generations in a SOC, the integrated phase jitter is more of a concern. For example, a PLL is generating a high speed sampling clock for an ADC as shown in Fig. 6.

Figure:5 Channel Corruption Due To LO Spur Tone



The Clock jitter causes a displacement of the precise sampling moment away from the ideal clock instance, and leads to a sampling error, which is proportional to the magnitude of the jitter and the slope of the continuous time signal. The SNR due to sampling jitter can be found as [10].

Figure:5 PLL Phase Noise Leads to Sampling Clock Jitter



4. Noise Sources in a PLL

As we have seen phase noise plays an important role in systems where PLLs are used. The most important noise sources in a PLL are the VCO noise and the reference noise. In addition, PFD, CP and the divider each contributes noise to the final clock. Fundamentally these are due to either thermal noise or 1/f noise. The effects of supply and substrate activity due to digital switching circuits are often treated as noise as well. In this subsection, we use the LTI model derived in section A to calculate the noise transfer function from each noise source to the PLL output [6], [11], [12]. The results provide important guidelines in process of making design tradeoffs. The LTI model from Fig.2 is remodeled with an explicit noise source added for the reference and the VCO. The VCO noise is modeled as the additive noise at the output. The transfer function from $\varphi_{n,vco}$ to φ_{out} is found to be:

$$\frac{\phi_{out}(s)}{\phi_{n,vco}(s)} = \frac{1}{1+G(s)} = \frac{sN}{sN + K_{PD} \cdot F(s) \cdot K_v} \tag{3}$$

Here the PD gain and loop filter gain are represented by K_{PD} and F(s) respectively. Similarly the transfer function from $\varphi_{n,ref}$ to φ_{out} is:

$$\frac{\phi_{out}(s)}{\phi_{n,ref}(s)} = \frac{G(s) \cdot N}{1+G(s)} = \frac{N \cdot K_{PD} \cdot F(s) \cdot K_v}{sN + K_{PD} \cdot F(s) \cdot K_v} \tag{4}$$

We can see the noise from VCO is high-pass filtered with pass band gain of 1 while the noise from reference is low-pass filtered with gain of N. For both the transition band edge is the PLL loop BW. The multiplication factor of N comes from the fact that output frequency is N times larger than the reference. For a free running VCO, the zero-crossing times follow a random walk process and the jitter referenced to a fixed starting point grows unbound with the measuring time interval. This is described in Fig. 7, where "v_n" represents the instantaneous device noise (both thermal noise and 1/f noise in nature) with a variance of σ_{n2} , referred to the input of VCO [5]. Jitter is measured at the output. Once the VCO is placed inside a PLL, as the time interval grows much larger than the

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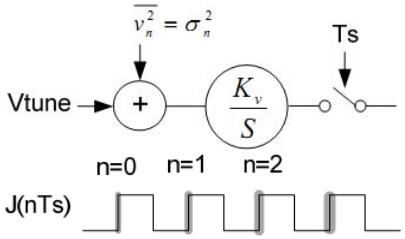
reciprocal of the PLL loop BW, the loop tracks out the cumulative jitter from VCO and the RMS jitter becomes bounded.

Figure:6 . Free Running VCO Noise



The noise of PD, CP, the LPF and the divider can also be analyzed by referring to either the reference node or the VCO node, and by use of the corresponding noise transfer function. The CP usually contributes little noise due to the small duty cycle factor in steady state. In steady state the UP and DN pulses from the PD are nearly equal and only last for a brief moment to switch the CP on. In our design, the minimum pulse width for UP and DN signals is about 200 ps. Only during this brief moment can the internal noise from the CP make it to the PLL output. Overall the effect is averaged out by the reference period [11].

The noise from the LPF and OPAMP also contribute to overall noise through various low- pass and band-pass functions and requires careful design tradeoffs. The LTI model is often used in practical PLL design and in analyzing phase noise and jitter. Phase noise is the frequency domain representation of random fluctuations in the phase angle; jitter is the time domain representation of essentially the same phenomena. In communication applications, phase noise limits the precision of a receive channel through reciprocal mixing. Distinctive spur tones can cause direct channel corruption.

III. MODIFIED MIXED SIGNAL PLL

The Mixed signal phase locked loop is a circuit that is made up of both analog and digital components. In this work modified architecture has phase frequency detector, voltage controlled oscillator as digital components and loop filter as analog component. Building blocks of mixed signal PLL are sequential phase detector, ring oscillator and operational amplifier based differential low pass filter.

1. Phase Frequency Detector

A usual PFD uses an asynchronous tri-state state machine implemented with two flip-flops. The built-in memory function allows the PD to detect frequency as well as phase. The schematic of proposed PFD composed of 24 transistors which we used for this work is shown in Fig. 8. A rising edge of the REFCLK triggers an UP pulse which is turned off only at the arrival of the next rising edge of FBCLK. Similarly a rising edge of the FBCLK triggers a DN pulse which is only turned off by the next arrival of the REFCLK.

The gates inserted in the reset path add a fixed delay which will cause an overlap at the end of the UP and DN pulses, where both are momentarily turned on. This removes the dead zone in the phase detector [13].It is important to keep both the UP and DN pulses with equal path delays. A transmission gate is also used to pad the path between UP and UPZ, and DN and DNZ.

Figure:7 Proposed Phase Frequency Detector with 24 Transistor

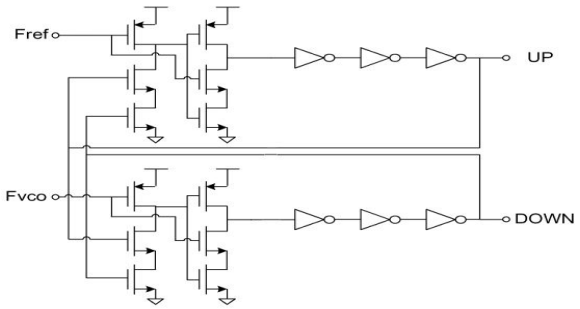


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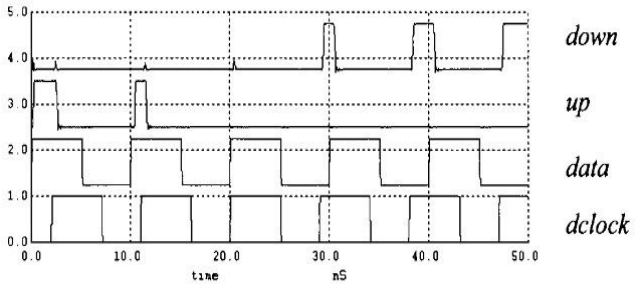
Figure:7 PFD Input and Output Waveforms

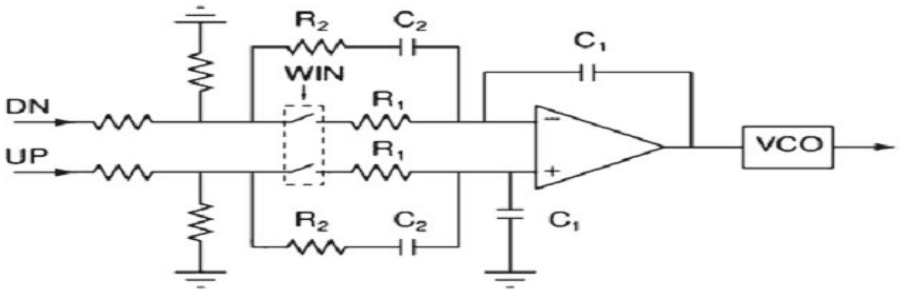


The PFD can be conveniently combined with a Charge pumps (CP) The UP and DOWN pulses are used to turn on and off a pair of switches that controls a pair of current sources in the CP. With arbitrary clock edges for REFCLK and FBCLK as illustrated in Fig 9.Note there is a brief overlapping period when both UP and DOWN are on. By sweeping one input clock against the other (both with equal frequency), we can see the linear range extends to from -2π to2π. Here, in this work PFD is connected directly to the differential low pass filter without any charge pump.

2. Active Loop Filter with Implicit Charge Pump

A second order active loop filter is used to implement a type II third order PLL [11]. Compared to the passive loop filter in Fig. 2, the active one provides additional isolation for the input node of VCO, and is in general more advantageous for spurious side bands. Both passive and active loop filters give identical transfer function. A well designed OPAMP should contribute minimum noise.

Figure:7 Differential Low Pass Filter with Implicit CP



Alternatively the loop filter can be implemented using an implicit CP [1]. This is shown in Fig. 10. This architecture was used in a 32 kHz reference PLL targeted for wireless connectivity and broadcast applications. While this architecture is functionally equivalent to the LPF, it allows for significant area savings by using a large R and moderate C for loop stabilization. The „windowing" concept was used to mitigate the problems of excessive thermal noise from the loop filter, as well as spurs from droop in the VCO control voltage due to leakage.

The importance of aforementioned architecture is UP and DN pulses do not operate any switches but are directly fed to the loop filter and that polarity of the UP and DN currents are the same .This helps to minimize mismatches between the UP/DN paths.

3. Voltage Controlled Oscillator

Ring oscillators are widely used in PLLs for their simplicity and smaller silicon area. The oscillator core consists of a chain of CMOS inverters forming a delay line. The frequency of oscillation is determined by the total phase shift of 360° at that frequency. Note that half the cycle delay is obtained through polarity inversion by using an

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odd number of inverters. Tuning is achieved by changing the current to charge the inverter parasitic capacitance, and this leads to a large tuning range.

A simple three stage inverter loop is used in the VCO design. The sizes of the transistors forming the ring which have a strong bearing on the phase noise and power consumption of the VCO have been optimized carefully [14], [15].

IV. RESULT AND DISCUSSION

Circuit level simulations were carried out in Mentor Graphics Pyxis with 180 nm technology. Conventional analog PLL was simulated in analog simulation mode and Mixed signal PLL was simulated in mixed signal mode. Noise analysis was done using an inbuilt noise analyzer tool. Noises at various parts of circuits like input, output portion and overall circuit were measured. Transient analysis was done for closed loop PLL. In this work delay parameters of the inverters are optimally chosen in such a way that ring oscillator to have 32 kHz free running frequency.

Figure:**8** Overall Output Waveforms of Mixed Signal PLL

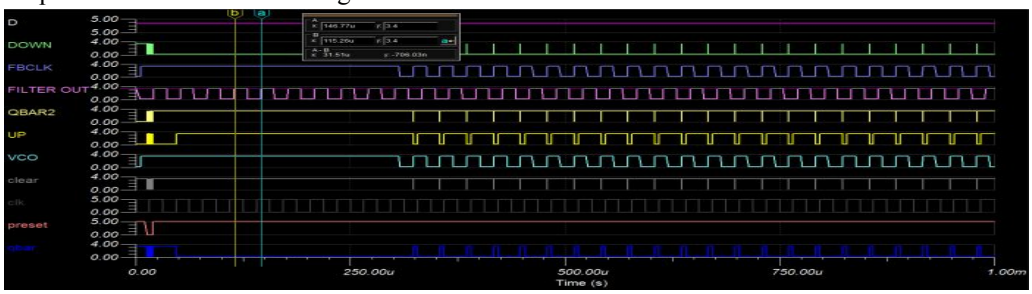


Figure:9 Mixed Signal PLL in a Locked

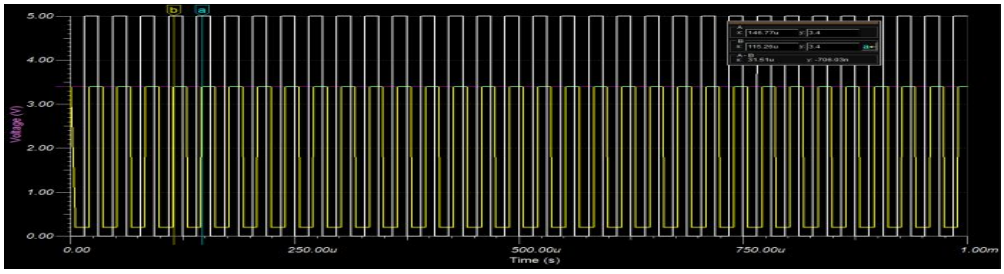
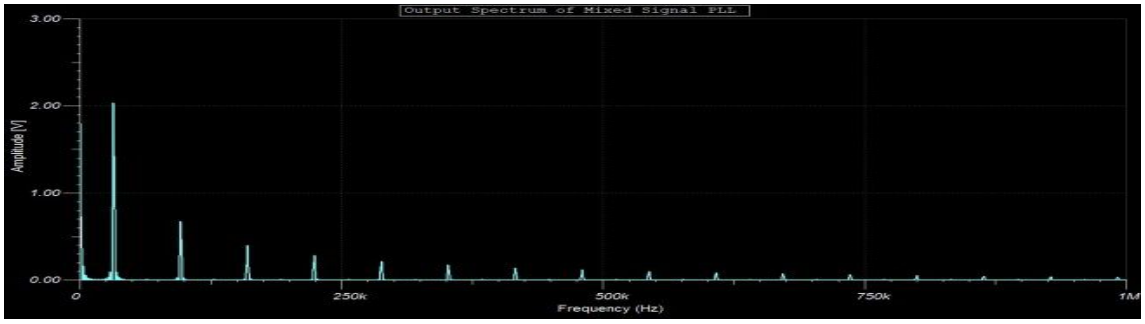


Figure:9 Spurious Performance of Proposed Mixed Signal PLL



From the above analysis results it is get to know that modified PLL has better SNR and less noise response compared to conventional PLL. Resistors and capacitors used in this design are also very less compared to previous PLL. Comparison of conventional PLL with modified one by means of various parameters at locked state is given in Table I.

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Table 9. Comparison of Plls at Locked State With 32 Khz Frequency

Parameter/Module	Analog PLL[1]	Modified Mixed Signal PLL (This work)
Max.Resistor	10 KΩ	500 Ω
Max.Capacitor	1 µF	10 pF
Overall noise	32 nV/Hz	30 nV/Hz
SNR	93 dB	152 dB
PFD	58 Transistors	24 Transistors
Ring Oscillators	3 Stages	5 Stages

V. CONCLUSION

The presented work analyzed the operation of a phase- locked loop and its different components. Two different architectures were implemented and simulated .In this work modified mixed signal PLL with 32 KHz frequency reference is compared with the conventional analog PLL of 32 KHz. From analysis results it is evident that major noise and spur causes like resistors and capacitors value considerably reduced in this design compared to conventional one. Since, it is tedious to control the switch dynamically in modified differential active low pass filter design window with fixed size is implemented by using a switch in SPICE tool. This work can be used for a FM receiver in portable applications. Since, it operates with 32 KHz reference frequency it consumes less power for operation. This is a desirable feature needed for battery operated devices such as mobile phones and tablets.

VI. ACKNOWLEDGMENT

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